ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device has first and second receivers and first and second transmitters. The first receiver has a first clock data recovery (CDR) circuit, and the second receiver has a second CDR circuit. Each of these first and second CDR circuits receives serial data, recovers a clock from the received serial data, and changes the phase of the generated clock. The first transmitter has a first serializer (SER), and the second transmitter has a second SER. The first SER converts parallel data into serial data synchronized with a transmit clock or the clock generated by the first CDR circuit. The second SER converts parallel data into serial data synchronized with a transmit clock or the clock generated by the second CDR circuit.